CURRICULUM VITAE

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CURRENT POSITION

Associate professor at DTU Compute, Technical University of Denmark.

EDUCATION

- **Ph.D. in Engineering,** September 1999.
  University of California, Irvine, USA.
- **M.S. in Electrical and Computer Engineering,** June 1995.
  University of California, Irvine, USA.
- **Eng. Degree *"Laurea"* in Electrical Engineering,** May 1988.
  University of Rome "La Sapienza", Roma, Italy.

EXPERIENCE

- **DTU Compute, Technical University of Denmark**, Kongens Lyngby, Denmark.
  Associate professor (May '03 - current).
- **Dept. of Electrical Engineering, University of Rome "Tor Vergata"**, Rome, Italy.
  Post-doc Researcher (Sept.'99 - May '03).
- **Dept. of Electrical & Computer Engineering, University of California**, Irvine, USA.
  Research Assistant (Jan.'94 - June'99)
- **Rockwell International, Multimedia Communications Division**, Newport Beach, USA.
  Summer Intern (July'95 - Sept.'95)
- **Ericsson Telecomunicazioni**, Rome, Italy.
  System & Software Engineer (Sept.'91 - Aug.'93)
- **STMicroelectronics** (formerly SGS-Thomson Microelectronics), Agrate Brianza, Italy.
  Design Engineer (Apr.'90 - Aug.'91)
- **Military Service in the Italian Army** (Mar.'89 - Mar.'90)
- **I.P.I.A. High School**, Orvieto, Italy.
  Teacher of digital and analog electronics. (Sept.'88 - Mar.'89)

RESEARCH AREAS

Arithmetic units and numerical processors

Hardware algorithms for numerical computations and their effective implementation in terms of speed of execution, area, and energy. Emphasys is given to more complicated operations such as division and square-root, and to the implementation of operations in decimal arithmetic.

Hardware acceleration on reconfigurable platforms
Design of Application Specific Processors (ASPs) for DSP and financial (decimal) applications. These ASPs can be implemented on FPGAs which can be fine tuned to match exactly the algorithm, and which are easy to reconfigure according to the application.

Power and thermal management of Systems-on-Chips
The main objective of this line of work is the study of techniques to reduce the power dissipation, without penalizing the performance, and to prevent the temperature to rise in excess. The power consumption reduction is carried out at different levels of abstraction.

Power efficient digital signal processors
Implementation of traditional DSP processors (filters, etc.) by using low-power methods to obtain significant reductions in power consumption. The main approaches are the use of residual arithmetic and trading off precision with power dissipation.

SUPERVISION OF Ph.D. STUDENTS

Wei Liu "Power and Thermal Management in System-on-Chips". DTU. 2007-2011.

Massimo Petricca (co-supervisor), Univ. of Rome Tor Vergata, Italy. 2008-2012.

Pietro Albicocco (co-supervisor), Univ. of Rome Tor Vergata, Italy. 2011-2014.

OTHER ACTIVITIES

- Associate Editor for *IEEE Transactions on Computers*, 2011–*current*
- Program Chair for *21st IEEE Symposium on Computer Arithmetic*, April 2013.
- Steering Committee Board member *IEEE Symposium on Computer Arithmetic*, 2015–i*current*
- Program Committee member of several international conferences.
- Reviewer for several conferences and journals.
- Manager of hardware labs at DTU Compute, 2004–*current*

SUMMARY OF PUBLICATIONS

	Quantity
Refereed international journals	9
Refereed proceedings of international conferences	63
Book chapters	5
Other publications	12

Indices from **Google Scholar** (04/12/2015) – http://scholar.google.dk/citations?user=BKgG5koAAAAJ&hl=en

citations	805
h-index	15
i10-index	27

PUBLICATIONS (complete list)

Journal Articles (Peer Review)

[1] A. T. Winther, W. Liu, **A. Nannarelli**, and S. Vrudhula. "Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation", *Microprocessors and Microsystems (MICPRO)*, vol. 39, n. 8, pp. 807-815, Nov. 2015.

[2] **A. Nannarelli**. "Performance/Power Space Exploration for Binary64 Division Units", *IEEE Transactions on Computers*, accepted. Published online DOI: 10.1109/TC.2015.2448097, June 2015.

[3] W. Liu, A. Calimera, A. Macii, E. Macii, **A. Nannarelli**, and M. Poncino, "Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 3, pp. 406-418, Mar. 2013.

[4] T. Lang and **A. Nannarelli**, "Comments on 'Improving the Speed of Decimal Division'", *IET Computers and Digital Techniques*, vol. 6, no. 6, pp. 370-371, 2012.

[5] W. Liu and **A. Nannarelli**. "Power Efficient Division and Square Root Unit", *IEEE Transactions on Computers*, vol. 61, no. 8, pp. 1059-1070, Aug. 2012.

[6] T. Lang and **A. Nannarelli**. "A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture", *IEEE Transactions on Computers*, June 2007. Vol. 56(6), p. 727-739, June 2007.

[7] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**. "Digit-Recurrence Dividers with Reduced Logical Depth", *IEEE Transactions on Computers*, Vol. 54, p. 837-851, July 2005.

[8] L. Benini, A. Macii, and **A. Nannarelli**. "A Code Compression Architecture for Cache Energy Minimization in Embedded Systems", *IEE Proceedings - Computers and Digital Techniques. Special Issue on Low-Power Systems-on-Chip*. Vol. 149, Iss. 4, p. 157-163, July 2002.

[9] **A. Nannarelli** and T. Lang. "Low-Power Divider", *IEEE Transactions on Computers*, Vol. 48, p. 2-14, Jan. 1999.

Conference Papers (Peer Review)

[1] G.C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration", *Proc. of IEEE International Symposium on Signal Processing and Information Technology (ISSPIT)*, Abu Dhabi, UAE, Dec. 2015

[2] **A. Nannarelli** , "Reliability in Warehouse-Scale Computing: Why Low Latency Matters", *Proc. of MEDIAN Finale, Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale*, Tallinn, Estonia, Nov. 2015.

[3] G.C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Characterization of RNS multiply-add units for power efficient DSP", *Proc. of 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Fort Collins, Colorado (USA), Aug. 2015.

[4] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, and M. Re, "Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives", *Proc. of the Int.l Symposium on Integrated Circuits (ISIC 2014)*, Singapore, Dec. 2014.

[5] J.K. Toft and **A. Nannarelli**, "Energy Efficient FPGA based Hardware Accelerators for Financial Applications", *Proc. of the 32nd Norchip Conference*, Tampere, Finland. Oct. 2014.

[6] **A. Nannarelli**, "Decimal Engine for Energy-Efficient Multicore Processors", *Proc. of the 22nd Int.l Conference on Very Large Scale Integration (VLSI-SoC)*, Playa del Carmen, Mexico, Oct. 2014.

[7] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Truncated Multipliers through Power-Gating for Degrading Precision Arithmetic", *Proc. of 47th Asilomar Conference on Signals, Systems, and Computers*. pp. 2172-2176, Pacific Grove (CA), USA, Nov. 2013.

[8] J. S. Hegner, J. Sindholt, and **A. Nannarelli**, "Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications", in *Proc. of the 30th Norchip Conference*, Copenhagen, Denmark, Nov. 2012.

[9] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Imprecise Arithmetic for Low Power Image Processing", *Proc. of 46th Asilomar Conference on Signals, Systems, and Computers*, pp. 983-987, Pacific Grove (CA), USA, Nov. 2012.

[10] M. Petricca, P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, and M. Re, "Power Efficient Design of Parallel/Serial FIR Filters in RNS", in *Proc. of 46th Asilomar Conference on Signals, Systems, and Computers*, pp. 1015-1019, Pacific Grove (CA), USA, Nov. 2012.

[11] A. Calimera, W. Liu, E. Macii, **A. Nannarelli**, and M. Poncino, "Power and Aging Characterization of Digital FIR Filters Architectures", *Proc. of the First Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12)*, Annecy, France, June 2012.

[12] **A. Nannarelli**, "FPGA Based Acceleration of Decimal Operations", *Proc. of International Conference on ReConFigurable Computing and FPGA's* , p. 146–151, Cancun, Mexico. 30 Nov.–2 Dec. 2011.

[13] A. T. Winther, W. Liu, **A. Nannarelli**, and S. Vrudhula, "Temperature Dependent Wire Delay Estimation in Floorplanning", *Proc. of 2011 Norchip Conference*, Lund, Sweden, 14–15 Nov. 2011.

[14] N. Borup, J. Dindrop, and **A. Nannarelli**, "FPGA Implementation of Decimal Processors for Hardware Acceleration", *Proc. of 2011 Norchip Conference*, Lund, Sweden, 14–15 Nov. 2011.

[15] P. Albicocco, G.C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Degrading precision arithmetics for low-power FIR implementation", *Proc. of 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, South Korea, 7-10 Aug. 2011.

[16] **A. Nannarelli**, "Radix-16 Combined Division and Square Root Unit", *Proc. of 20th IEEE Symposium on Computer Arithmetic*, p. 169–176, Tubingen, Germany, 25–27 July 2011.

[17] W. Liu and **A. Nannarelli**, "Temperature Aware Power Optimization for Multicore Floating-Point Units", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 1134-1138, Pacific Grove (CA), USA, Nov. 2010.

[18] G.C. Cardarilli, **A. Nannarelli**, Y. Oster, M. Petricca, and M. Re, "Design of Large Polyphase Filters in the Quadratic Residue Number System", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 410-413, Pacific Grove (CA), USA, Nov. 2010.

[19] M. Petricca, G.C. Cardarilli, **A. Nannarelli**, M. Re, and P. Albicocco, "Degrading Precision Arithmetic for Low Power Signal Processing", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 1163-1167, Pacific Grove (CA), USA, Nov. 2010.

[20] W. Liu and **A. Nannarelli**, "Power Dissipation Challenges in Multicore Floating-Point Units", *Proc. of 21st IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010)*, p. 257-264, Rennes, France, July 2010.

[21] W. Liu, A. Calimera, **A. Nannarelli**, E. Macii, and M. Poncino, "Post-placement Temperature Reduction Techniques", *Proc. of 2010 Design Automation and Test in Europe Conference (DATE 2010)*, p. 634-637, Dresden, Germany, Mar. 2010.

[22] S. Gonzalez-Navarro, **A. Nannarelli**, C. Tsen, and M. J. Schulte, "Combined Decimal and Binary Floating-point Divider", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 930-934, Pacific Grove (CA), USA, Nov. 2009.

[23] M. Petricca, H. Li, S. Forchhammer, **A. Nannarelli**, M. Re, J. D. Andersen, and G.C. Cardarilli, "Hardware Implementation of Real-Time MPEG Analysis and Deblocking for Video Enhancement", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 754-758, Pacific Grove (CA), USA, Nov. 2009.

[24] I. Shuli, M. Petricca, G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Multiple Constant Multiplication through Residue Number System", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 736-739, Pacific Grove (CA), USA, Nov. 2009.

[25] **A. Nannarelli**, "Low Power Hardware Platforms", *Proc. of 12th International Symposium on Wireless Personal Multimedia Communications (WPMC'09)*, Sendai, Japan. Sep. 7-10, 2009.

[26] W. Liu, A. Calimera, **A. Nannarelli**, E. Macii, and M. Poncino, "On-chip Thermal Modeling Based on SPICE Simulation", *Proc. of 19th International Workshop on Power And Timing Modeling, Optimization and Simulation PATMOS 2009*, p. 66-75. Delft, Netherlands, Sep. 2009.

[27] T. Lang and **A. Nannarelli**, "Division Unit for Binary Integer Decimals", *Proc. of 20th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP '09)*, p. 1-7, Boston, USA, 7-9 July 2009.

[28] W. Liu and **A. Nannarelli**, "Net Balanced Floorplanning Based on Elastic Energy Model", *Proc. of 26th Norchip Conference*, p. 258-263, Tallinn, Estonia, Nov. 2008.

[29] W. Liu and **A. Nannarelli**, "Power Dissipation in Division", *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 1790-1794, Pacific Grove (CA), USA, Oct. 2008.

[30] **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Reducing Power Dissipation in Pipelined Accumulators", *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 2098-2101, Pacific Grove (CA), USA, Oct. 2008.

[31] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters", *Proc. of 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, p. 37-41, Rodos, Greece, Oct. 2008.

[32] L. Dadda and **A. Nannarelli**, "A Variant of a Radix-10 Combinational Multiplier", *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3370-3373, Seattle, USA, May 18-21, 2008.

[33] G.C. Cardarilli, L. Di Nunzio, **A. Nannarelli**, and M. Re. "ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations", *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3434-3437, Seattle, USA, May 18-21, 2008.

[34] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Residue Number System for Low Power DSP Applications", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1412-1416, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[35] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Impact of RNS Coding Overhead on FIR Filters Performance", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1426-1429, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[36] T. Lang and **A. Nannarelli**, "Combined radix-10 and radix-16 division unit", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 967-971, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[37] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low-power adaptive filter based on RNS components ", *Proc. of 2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3211-3214, New Orleans, USA, May 28-31, 2007

[38] T. Lang and **A. Nannarelli**, "A Radix-10 Combinational Multiplier", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 313-317, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[39] **A. Nannarelli**, M.S. Rasmussen, and M.B. Stuart, "A 1.5 GFLOPS Reciprocal Unit for Computer Graphics", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1682-1686, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[40] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re. "A hybrid RNS adaptive filter for channel equalization", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1706-1710, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[41] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low Power and Low Leakage Implementation of RNS FIR Filters", *Proc. of 39th Asilomar Conference on Signals, Systems, and Computers*, p. 1620-1624, Pacific Grove (CA), USA, Oct. 30 – Nov. 2, 2005.

[42] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**, "Low Latency Digit-Recurrence Reciprocal and Square-Root Reciprocal Algorithm and Architecture", *Proc. of 17th Symposium on Computer Arithmetic*, p. 147-152, Cape Cod, USA, June 27-29, 2005.

[43] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Programmable Power-of-two RNS Scaler and its Application to a QRNS Polyphase Filter", *Proc. of 2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 1002-1005, Kobe, Japan, May 23-26, 2005.

[44] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low-Power Implementation of Polyphase Filters in Quadratic Residue Number System", *Proc. of 2004 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 725-728, May 23-26, 2004.

[45] A. Del Re, **A. Nannarelli**, and M. Re, "A tool for automatic generation of RTL-level VHDL description of RNS FIR filters", *Proc. of 2004 Design, Automation and Test in Europe Conference* (DATE), Vol. 48, p. 686-687, Paris, France, Feb. 16-20, 2004.

[46] **A. Nannarelli**, G.C. Cardarilli, and M. Re, "Power-delay tradeoffs in residue number system", *Proc. of 2003 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. V, p. 413-416, May 25-28, 2003.

[47] G.C. Cardarilli, A. Del Re, R. Lojacono, **A. Nannarelli**, and M. Re, "RNS implementation of high performance filters for satellite demultiplexing", *Proc. of the 2003 IEEE Aerospace Conference*, Vol. 3, p. 1365-1379, Mar. 8-15, 2003.

[48] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**, "Fast Radix-4 Retimed Division with Selection by Comparisons", *Proc. of IEEE 13th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2002)*, p. 185-196, San Jose (CA), USA, July 17-19, 2002.

[49] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Residue Number System Reconfigurable Datapath", *Proc. of 2002 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 756-759, Phoenix, Arizona, USA, May 2002.

[50] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Power Characterization of Digital Filters Implemented on FPGA", *Proc. of 2002 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. V, p. 801-804, Phoenix, Arizona, USA, May 2002.

[51] A. Del Re, **A. Nannarelli**, and M. Re, "Implementation of Digital Filters in Carry-Save Residue Number System", *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1309-1313, Pacific Grove (CA), USA, Nov. 2001.

[52] A. Del Re, **A. Nannarelli**, and M. Re, "Fast Prototyping Techniques Applied to the Hardware Simulation of Telecommunication Systems", *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1314-1317, Pacific Grove (CA), USA, Nov. 2001.

[53] **A. Nannarelli**, M. Re, A. Del Re, G.C. Cardarilli, and R. Lojacono, "High Speed RNS A/D Front End", *Proc. of 6th Euro Workshop on ADC Modelling and Testing*, p. 19-22, Lisbona, Portugal, Sep. 2001.

[54] L. Benini, A. Macii, and **A. Nannarelli**, "Cached-Code Compression for Energy Minimization in Embedded Processors", *Proc. of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 322-327, Huntington Beach, California, USA, Aug. 2001.

[55] **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Tradeoffs between Residue Number System and Traditional FIR Filters", *Proc. of IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 305-308, Sydney, Australia, May 2001.

[56] M. Re, **A. Nannarelli**, G.C. Cardarilli, and R. Lojacono, "FPGA Implementation of RNS to Binary Signed Conversion Architecture", *Proc. of IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. IV, p. 350-353, Sydney, Australia, May 2001.

[57] A. D'Amora, **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Reducing Power Dissipation in Complex Digital Filters by using the Quadratic Residue Number System", *Proc. of 34th Asilomar Conference on Signals, Systems, and Computers*, p. 879-883, Pacific Grove (CA), USA, Nov. 2000.

[58] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Reducing Power Dissipation in FIR Filters using the Residue Number System", *Proc. of 43rd IEEE Midwest Symposium on Circuits and Systems*, p. 320-323, Lansing, USA, Aug. 2000.

[59] **A. Nannarelli** and T. Lang, "Low-Power Radix-4 Combined Division and Square Root", *Proc. of IEEE International Conference on Computer Design* (ICCD), p. 236-242, Austin, Texas, USA, Oct. 1999.

[60] **A. Nannarelli** and T. Lang, "Low-Power Division: Comparison among implementations of radix 4, 8 and 16". *Proc. of 14th Symposium on Computer Arithmetic*, p. 60-67, Adelaide, Australia, Apr. 1999.

[61] **A. Nannarelli** and T. Lang, "Low-Power Radix-8 Divider", *Proc. of IEEE International Conference on Computer Design* (ICCD), p. 420-426, Austin, Texas, USA, Oct. 1998.

[62] **A. Nannarelli** and T. Lang, "Power-Delay Tradeoffs for Radix-4 and Radix-8 Dividers", *Proc. of International Symposium on Low Power Electronics and Design* (ISLPED), p. 109-111, Monterey, California, USA, Aug. 1998.

[63] **A. Nannarelli** and T. Lang, "Low-Power Radix-4 Divider", *Proc. of International Symposium on Low Power Electronics and Design* (ISLPED), p. 205-208, Monterey, California, USA, Aug. 1996.

Book Chapters

[1] P. Montuschi, **A, Nannarelli**. "Division Algorithms for Digital Arithmetic", *Encyclopedia of Computer Science and Technology*. CRC Press - Taylor and Francis Group, New York. (In Press)

[2] W. Liu, **A. Nannarelli**. "Power and Thermal Efficient Numerical Processing", *Handbook on Data Centers*, p. 263-286. Springer, New York (USA), 1st Edition, 2015. ISBN 978-1-4939-2091-4

[3] G.C. Cardarilli, **A. Nannarelli**, M. Re. "On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters", *VLSI-SoC: Design Methodologies for SoC and SiP*, p. 174-190. Springer, 1st Edition, 2010. ISBN: 978-3-642-12266-8

[4] **A. Nannarelli**. "Low Power Hardware Platforms", *Towards Green ICT*, p. 131-143. River Publishers, Aalborg, Denmark. 2010. ISBN 978-87-92329-34-9.

[5] R. Lojacono, G.C. Cardarilli, **A. Nannarelli** and M. Re. "Residue Arithmetic Techniques for High Performance DSP", Problems in Modern Applied Mathematics, World Scientific Engineering Society Press, p. 314-318, Sep. 2000.

Other Publications

Partial list. Technical reports not listed.

[1] A. Nannarelli, P. Seidel and P.T.P. Tang, "Guest Editors' Introduction: Special Section on Computer Arithmetic", *IEEE Transactions on Computers*, vol. 63, no. 8, pp. 1852-1853, Aug. 2014.

[2] L. Dadda and A. Nannarelli. "Fast Multi Operand Decimal Adders using Digit Compressors with Decimal Carry Generation", *Rendiconti - Accademia Nazionale delle Scienze detta dei XL. Memorie di Scienze Fisiche e Naturali*, serie V, vol. XXXII, parte II, p. 47-81, 2008.

[3] A. Nannarelli. "Low-Power Division and Square Root", Ph.D. Dissertation, University of California, Irvine, June 1999.

[4] A. Nannarelli. "Power Evaluation Tool: modeling and implementation", COMPASS User's Group Conference, San Jose, CA, Apr. 1996.

[5] A. Nannarelli. "Implementation of a Radix-512 Divider", M.S. Thesis, University of California, Irvine, June 1995.

[6] A. Nannarelli and T. Lang. "Implementation of Division and Square Root: Modeling and Evaluation", Final Report for MICRO Project #94-070, University of California, 1995.

[7] A. Nannarelli and T. Lang. "Implementation of Division with Prescaling: Modeling and Evaluation", Final Report for MICRO Project #93-088, University of California, 1994.